Course Type	Course Code	Name of Course	L	T	P	Credit
DP	NECC527	HDL-based System Design Lab	0	0	3	1.5

Course Objective
The objective of this lab is to describe the simulation and synthesis of digital systems using Hardware Description Languages (HDL) and explain its various abstraction levels
Learning Outcomes
By the end of the course, the student must be able to: • Write efficient hardware designs in VHDL/Verilog and perform high-level HDL simulation. • Carry out basic digital design flows. • Explain different levels of abstraction with the programming examples.

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Introduction to VHDL; Familiarization with EDA tools for VLSI: Xilinx ISE Design Suite/Vivado; Digital design using FPGAs; Introduction to simulation and synthesis	9	To learn the programing aspects of hardware description language and its significance in programmable logic design flow
2	Simple combinational circuit design with VHDL/Verilog: Basic gates, Half and Full adder, multiplexer, decoders, tri-state gates and so on; Design of: 4-bit parallel adder and subtractor, BCD Adder, multiplier; Design of latches and flip-flops and sequential circuits.	18	Develop skill to design various digital circuits with HDL and simulate their performance. The students also realizes how a design transforms into target technology
3	Introduction to HDL Test Benches; Test Bench-based digital design verification of basic combinational circuits	9	To develop circuit specific simulators.
4	Design of small-scale practical systems, such as, Package sorter/Traffic Light Controller/ALU	6	Utilize the skills in HDL to design a minor project
	Total	**42**	

Text Books:

1. Perry DL. VHDL: Programming by example. New York: McGraw-Hill; 2002 May 12.

Reference Books:

1. Lab Manual on HDL-based System Design Lab